This application is a continuation application of United States Patent Application entitled " Multi-Directional Wiring On A Single Metal Layer " filed on December 6, 2000, and having the Serial No. 09/733,104.

IN THE CLAIMS:

Please amend claims 16 and 28 as follows:

16. (Once Amended) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in an integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors, and said self contained layout section comprising a routing of conductors, for a portion of said metal layer, developed independent from routing of conductors for circuits in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout section.

28. (Once Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors, for a portion of said metal layer, developed independent from routing of conductors for circuits in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout.

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Overview of the Claimed Invention:

An integrated circuit employs diagonal wiring geometries to provide noise immunity from self contained layout sections. A self contained layout section, or pre-